IN THE SPECIFICATION:

Insert the heading before the paragraph beginning at page 1, line 9 as follows:

1. Field of the Invention

Insert the heading before the paragraph beginning at page 1, line 13 as follows:

2. Description of the Related Art

Paragraph beginning at page 1, line 18 has been amended as follows:

A first drive signal SG1 of the control circuit 2 is supplied to the gate of the main switching element 3, which is an enhancement-type N-channel MOS transistor. The switching element 3 operates as a main switch for driving a load. The drain of the switching element 3 is supplied with a supply voltage Ve from a battery, while the source of the switching element 3 is connected to the drain of the synchronous switching element 4, which is an enhancement-type N-channel MOS transistor. The gate of the synchronous switching element 4 is supplied with a second drive signal SG2 of the control circuit 2, while the source thereof is connected to [[the]] ground GND.

Paragraph beginning at page 3, line 25 has been amended as follows:

The pulse signal S3 is supplied to the inverter circuit 21, which in turn supplies an inverted signal of the pulse signal S3 to the gate of the N-channel MOS transistor T1. The source

of the transistor T1 is connected to the ground GND and the drain thereof is connected to the current source 26. A node between the transistor T1 and the current source 26 is connected via the inverter circuit 22 to the inverter circuit 23, which outputs the first control signal S4, and also to [[the]] ground GND via the capacitor C1.

Paragraph beginning at page 4, line 2 has been amended as follows:

As shown in Fig. 3, when the pulse signal S3 rises, an input signal S6 of the inverter circuit 22 also rises in accordance with a current I1 from the current source 26 and a capacitance of the capacitor C1. Subsequently, when the pulse signal S3 falls, the transistor T1 is turned ON, thus causing the input signal S6 to fall rapidly. When the voltage of the input signal S6 exceeds a threshold voltage Vth of the inverter circuit 22, the inverter circuit 22 inverts the input signal S6. Therefore, the first control signal S4 rises as delayed with respect to the rising timing of the pulse signal S3 by time td1 which corresponds to the charging time of the capacitor C1 and falls substantially at the same time as the pulse signal S3 falls. The delay time td1 is obtained by:

$$td1 = Vth*C1/I1$$